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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,176	06/30/2003	Steven H. Voldman	BUR920030009US1	1175
21918	7590	02/07/2005	EXAMINER KITOV, ZEEV	
DOWNS RACHLIN MARTIN PLLC 199 MAIN STREET P O BOX 190 BURLINGTON, VT 05402-0190			ART UNIT 2836	PAPER NUMBER

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/604,176

Applicant(s)

VOLDMAN, STEVEN H.

Examiner

Zeev Kitov

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on November 23, 2004. Claims 1, 2, 7, 8, 12 and 13 are amended.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 3 and 9 recite limitation "said voltage potential". There is insufficient antecedent basis for these limitations in the claims.

Objection

Claims 7, 9, 12 and 17 are objected, since Applicant uses the term "active clamp network". Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "active clamp network" in claims 7, 9, 12, and 17 is used by the claims to mean "switching off network", while the accepted meaning is "a circuit

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that adds a fixed bias to a wave at each occurrence of some predetermined feature of the wave so that the voltage or current of the feature is held at, or “clamped” to some specified level.” (The Authoritative Dictionary of IEEE Standard Terms, 7th Ed., 2000). The term is indefinite because the specification does not clearly redefine the term.

For purpose of examination, the claims limitations are interpreted as “switching off network”.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,624,660) in view of Lin et al. (US 6,473,282) and Miyamoto (US 4,905,199). Li et al. disclose following elements of Claim 1 including an integrated circuit having: a substrate (P-SUB in Fig. 2B), a power rail (Vss in Fig. 3) and a latchup control isolation network electrically coupled to the substrate, the latchup control isolation network adapted to electrically isolate the circuit from the power rail (col. 6, lines 36 – 67). It further discloses an active clamp network (elements 58, 64 and 52 in Fig. 3). However, it does not disclose isolating a sea of gates. Lin et al. disclose a sea of gates (elements 1 and 2 in Fig. 1, 8, 9, 10)

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being isolated by the latchup control isolation network (elements 3, 31 and 32 in Fig. 3). Both references have the same problem solving area, namely providing the latchup isolation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Li et al. solution by adding the sea of gates according to Lin et al., because as well known in the art, in modern electronics the circuit block include plurality of gates; so the latchup protection circuit should being able to isolate the whole block with plurality of gates. As to the claim limitation: "isolating sea of gates from said power supply in response to latchup event on said substrate", Miyamoto discloses (see fig. 13A and 13B, col. 6, line 3 – col. 7, line 9) that any latchup event involves flowing of substantial currents in the substrate and development of noticeable voltage drops in the substrate. Therefore, involvement of substrate in the latchup events is inherent in the latchup effect.

Claims 7, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Lin et al. and Miyamoto and Blossfeld et al. (US 5,530,394). Claims 7 and 12 differ from Claim 1 rejected accordingly by their limitations of an active switching off network. Blossfeld et al. disclose the active switching off network (elements T14, T7, T9, T11, nD in Fig. 8, col. 6, line 39 – col. 7, line 37) connected to the substrate (see Fig. 5). It further discloses turning off the latchup control isolation network, when connected in the prior step, thereby isolating the power rail from the protected circuit (col. 6, line 39 – col. 7, line 37). Both references have the same problem solving area, namely providing the latchup protection to the circuit (see col. 7, line 64 – col. 8, line 2 in Blossfeld

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et al.). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by adding the switching off circuit of Blossfeld et al., because as Blossfeld et al. state (col. 1, lines 11 – 31, col. 7, line 64 – col. 8, line 2), such solution provides the latchup protection to the system having multiple voltage supply sources.

Regarding Claims 3, 9, 14 and 17, Li et al. disclose the latchup control isolation network being turned off thereby isolating the protected circuit block from the power rail when the voltage potential equals or is greater than a first predetermined value (col. 6, lines 36 – 67).

Regarding Claims 4, 10, 15 and 18, Li et al. disclose the first predetermined value as being $V_{dd} + V_{be}$ (col. 6, lines 5 – 15).

Regarding Claims 5, 11, 16 and 19, the explanation given by Li et al. (col. 6, lines 5 – 15) regarding the NMOS transistor (element 14 in Fig. 2A and B) can be extended to the PMOS transistor (element 12 in Fig. 2A and B) with changing $V_{dd} + V_{be}$ to $V_{ss} - V_{be}$ due to well known in the art mirror identity of NMOS/PMOS, NPN/PNP schematics. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by adding the second predetermined value of $V_{ss} - V_{be}$ for protection against latchup developing from the PNP parasitic transistor, because as well known in the art, due to the mirror identity of NMOS/PMOS, NPN/PNP schematics the same considerations of the latch up process initiation are valid for PNP parasitic transistor with V_{ss} voltage playing the same role as V_{dd} for NPN transistor.

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Regarding Claim 6, Li et al. disclose the latchup control isolation network including the inverter circuit (element 64 in Fig. 3 playing the role of inverter with regard to element 52).

Regarding claims 2, 8 and 13, Blossfeld et al. disclose the substrate having a first polarity (substrate p- in Fig. 5), the circuit including a well having a second polarity (n- and n+ wells in Fig. 5). Even though the Fig. 5 does not show a whole latchup protection circuit, by a way of analogy, it is implicitly suggested that the circuit of Fig. 8 is designed the same way, i.e. the latchup control isolation circuit is also electronically coupled to the wells shown in Fig. 5 and is adapted to electrically isolate the circuit from the power rail in response to latchup events on the substrate (col. 7, line 64 – col. 8, line 2, col. 6, line 39 – col. 7, line 25). The sea of gates is disclosed by Miyamoto and isolating by the switch off circuit is disclosed by Blossfeld et al. (see rejection of Claim 1 above). The motivations for modification of the primary references are the same as above.

Response to Arguments

Applicant's Arguments have been given careful consideration but they are now moot in view of new ground of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

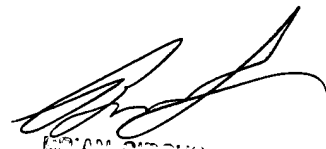
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See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
01/26/2005



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